

Number of traps and trap depth position on statistical distribution of random telegraph noise in scaled NAND flash memory

Toshihiro Tomita and Kousuke Miyaji

Department of Electrical and Electronic Engineering, Shinshu University, Nagano 380-8553, Japan

E-mail: kmiyaji@shinshu-u.ac.jp

Abstract

The dependence of random telegraph noise (RTN) amplitude distribution on the number of traps and trap depth position is investigated using three-dimensional Monte Carlo device simulation including random dopant fluctuation (RDF) in a 30 nm NAND multi level flash memory. The ΔV_{th} tail distribution becomes broad at fixed double traps, indicating that the number of traps greatly affects the worst RTN characteristics. It is also found that for both fixed single and fixed double traps, the ΔV_{th} distribution in the lowest cell threshold voltage (V_{th}) state shows the broadest distribution among all cell V_{th} states. This is because the drain current flows at the channel surface in the lowest cell V_{th} state, while at a high cell V_{th} , it flows at the deeper position owing to the fringing coupling between the control gate (CG) and the channel. In this work, the ΔV_{th} distribution with the number of traps following the Poisson distribution is also considered to cope with the variations in trap number. As a result, it is found that the number of traps is an important factor for understanding RTN characteristics. In addition, considering trap position in the tunnel oxide thickness direction is also an important factor.

1. Introduction

Random telegraph noise (RTN) becomes one of the main causes of error in the latest flash memory technology.¹⁻¹⁰⁾ RTN is a time-domain drain current I_D or V_{th} fluctuation induced by the emission/capture of a single electron at a tunnel oxide trap during read operation, as shown in Fig. 1.²⁻⁵⁾ RTN amplitude (ΔV_{th}) and its statistical variation becomes worse in advanced flash memories since single-electron behavior largely affects cell characteristics as the capacitance of a floating-gate (FG)-type NAND flash memory cell is reduced.¹¹⁻¹⁵⁾ It is important to clarify the physical origins and the contributions of RTN statistical characteristics to improve statistical model accuracy.

In our previous work,¹⁶⁾ ΔV_{th} distributions considering a fixed single trap were studied focusing on substrate doping concentration N_A in a 30 nm NAND flash memory by three-dimensional (3D) Monte Carlo device simulation, as shown in Figs. 2(a) and 2(b). In this simulation random dopant fluctuation (RDF) is also considered by including atomistic doping.¹⁷⁻²⁰⁾ A single electron was randomly located at the channel surface as a trap with widely varying N_A from 1×10^{17} to 3×10^{18} cm⁻³. The statistical model of the RTN in a NAND flash memory is also considered for comparison, which was given by Fukuda et. al. based on the measurement results used for solving Eqs. (1) and (2),¹⁾

$$f(\Delta V_{th}) = \frac{1}{\sigma} \cdot \exp\left(\frac{-\Delta V_{th}}{\sigma}\right) \quad (1)$$

$$\sigma = \alpha \cdot \frac{t_{ox}}{\sqrt{L_{eff}W_{eff}}} \cdot N_A^{0.6} \text{ (V)} \quad (2)$$

where t_{ox} , N_A , L_{eff} , and W_{eff} are oxide thickness, channel doping concentration and effective channel length and width, respectively. The parameter α is determined by fitting using the measured RTN data.¹⁾ This model considers the effect of the RDF in Eq. (2). From the 3D device simulation results in Fig. 2(a), no ΔV_{th} tail distribution is observed in the high- ΔV_{th} region when N_A is low here and for all ranges (1×10^{17} - 1×10^{18} cm⁻³). While the tail is observed at a high N_A (3×10^{18} cm⁻³), as shown in Fig. 2(b). Considering that a low N_A is required for NAND flash memories to prevent the leakage current between p-n junctions in the program inhibit cells²¹⁻²³⁾. The RTN distribution obtained by the 3D Monte Carlo device simulation underestimates the tail distribution in an actual NAND flash memory by simply considering RDF and a single trap. Therefore, to understand the details of the RTN

characteristics, other factors should be considered at a low N_A . In this work, ΔV_{th} distributions in a 30 nm 2 bit/cell multi level cell NAND flash memory architecture are investigated focusing on the number of traps and trap depth position. Here, three kinds of policies are considered for the number of traps used in this simulation: fixed single trap, fixed double traps, and Poisson distribution.¹⁾

This paper is organized as follows. In Sect. 2, device simulation conditions are explained. In Sect. 3, we show and discuss the results of the number of traps and trap depth position dependence of ΔV_{th} distribution for each cell V_{th} state. Finally, conclusions are given in Sect. 5.

2. 3D device simulation conditions

A 30 nm, 2 bit/cell NAND flash memory cell structure is adopted for 3D device simulation used in this work, as shown in Fig. 3(a).¹⁶⁾ The coordinates of the channel length, width, and cell height directions are defined as x, y and z respectively, as shown in this figure. Figures 3(b) and 3(c) show the cross-section views of the x-z and y-z planes, respectively. The SiO₂ tunnel oxide thickness t_{ox} , inter-poly dielectric thickness t_{IPD} , and floating gate (FG) height t_{FG} are 7, 10, and 80 nm, respectively.⁸⁾ Both the channel width W and length L_g are set at 30 nm, and the source/drain junction depth x_j is set at 10 nm. N_A is $3 \times 10^{17} \text{ cm}^{-3}$ while the punch-through stopper (PTS) layer is adopted at 30 nm below the source/drain junction to suppress the excess-short-channel effect.²⁴⁻²⁸⁾ The PTS doping concentration is $9 \times 10^{17} \text{ cm}^{-3}$.

Figure 4 shows the four cell V_{th} state distributions of the 2 bit/cell MLC architecture²⁹⁾ in this work. Cell V_{th} is controlled by changing the initial amount of charges of FG. The range of V_{th} values is from -2.5 to 3.5 V. The cell V_{th} state “11” is the lowest cell V_{th} state corresponding to the erase state, and cell V_{th} state “10” is the highest cell V_{th} state. Over 100 NAND flash cells with an atomistic doping profile¹⁷⁻²⁰⁾ and traps are prepared by Monte Carlo simulation. To emulate the trapped states, a $1 \times 1 \text{ nm}^2$ negative surface charge is randomly placed at the channel surface (tunnel oxide/substrate interface) whose charge amount is equals to that of a single electron. V_{th} is defined as the V_{CG} value when I_D reaches $W/L_g \times 10^{-7} \text{ A}$. ΔV_{th} is obtained by subtracting V_{th} in detrapped state from that in trapped state for each cell V_{th} state. Here, atomistic doping profiles are the same for both

the trapped and detrapped states. As can be understood from this simulation procedure, the trap energy levels are not considered for simplicity.^{3,10)} Three cases are assumed for the number of traps used in the Monte Carlo simulation: the fixed single trap, fixed double traps, and Poisson distribution. Cells without traps can be considered for the Poisson distribution where the number of traps is generated along the Poisson distribution. In this case, two trap densities (N_{trap}) are considered, 2×10^{10} and 2×10^{11} cm⁻² for the low and high trap densities, respectively. Figure 5 shows the probability of the number of traps for each N_{trap} . In this work, the RTN model¹⁾ is used for comparison based on Eqs. (1) and (2) with the device parameters used in this work.

3. Simulation results and discussions

Figures 6(a) and 6(b) show ΔV_{th} distributions with fixed single trap and double traps cases for each cell V_{th} state. Again, for the single trap, ΔV_{th} tails of all cell V_{th} states are not broad in the high- ΔV_{th} region, indicating that for the single trap is underestimation the distribution compared with the measurement-based RTN model. On the other hand, for the double traps, the ΔV_{th} tail distributions of all cell V_{th} states are broad, which shows a similar trend in the high- ΔV_{th} region to the RTN model. Another discrepancy between the 3D device simulation and the RTN model results is that the average ΔV_{th} of the 3D device simulation is much higher than that of the RTN model. This is because all the simulated cells contain RTN traps while cells without RTN traps are the majority actually. Finally, Figs. 6(a) and 6(b) shows that the ΔV_{th} distribution of the lowest cell V_{th} state (state“11”) for both single and double traps is the broadest among all of the cell states. In order to explain these results, current distributions near cell V_{th} at the center of the channel surface ($x = 0$ nm) for each cell V_{th} state are investigated, which are shown in Figs. 7(a) and 7(b). As stated in Sect. 2, the amount of channel current near cell V_{th} is the same for all cell V_{th} states because V_{th} is defined as the V_{CG} value when I_{D} reaches $W/L_{\text{g}} \times 10^{-7}$ A. From Fig. 7(a), at a low cell V_{th} , current concentrates at the center of the channel surface because the coupling between FG and the channel is dominant. On the other hand, as the cell V_{th} increases, current flows at both channel edges since the coupling between CG and the channel gradually becomes dominant.³⁰⁾ Moreover, the channel depth dependence on channel current density for each cell V_{th} state are shown in Figs. 8(a) and 8(b). The

horizontal y -axis is the channel width direction, as shown in Figs. 7(a) and 7(b). The black plot shows the channel current at the channel surface ($z = -1$ nm) and the blue one shows that at 7 nm below the channel surface. From Fig. 8(a), it is found that almost all of the channel currents flow at the channel surface at the low cell V_{th} state. On the other hand, the channel current at the high cell V_{th} is less dependent on the channel depth owing the fringing coupling from the CG. Therefore, since the traps are located at the channel surface in this simulation, a high ΔV_{th} tends to exist at the low cell V_{th} . Figures 9(a) and 9(b) show ΔV_{th} against trap position along y with double traps for the lowest and highest cell V_{th} states, respectively. Here, the same atomistic channel doping is used in both Figs. 9(a) and 9(b). The horizontal axis y_1 shows the trap location along y , and vertical axis y_2 shows the other trap location. From Fig. 9(a), the high- ΔV_{th} region at the lowest cell V_{th} is broader than that at the highest cell V_{th} . Also, from this result, it is found that a high ΔV_{th} occurs at the lowest cell V_{th} in this work.

Figures 10(a) and 10(b) show the ΔV_{th} distributions for the Poisson distribution with the cell V_{th} states “11” and “10” for the low and high N_{trap} values, respectively. In these figures, the average ΔV_{th} is closer to the measurement-based model for the Poisson distribution compared with the fixed trap number in Figs. 6(a) and 6(b), since the cells without RTN is included in this trap case. It can also be seen that the simulated distribution seems to be the combination of the distributions of the single trap and double traps from Fig. 10(a) at a low N_{trap} where the distribution of the single trap is predominant in the low- ΔV_{th} region while that of the double traps is predominant in the high- ΔV_{th} region. On the other hand, the ΔV_{th} distribution at a high N_{trap} in Fig. 10(b) shows wide variations compared with the RTN model since a significant number of cells contain more than two traps, as shown in Fig. 5(b). However, this result obviously overestimates the ΔV_{th} distribution since not all of the traps will contribute to RTN, as is the case in this simulation. Although there are rooms for the 3D device simulation to reproduce the measurement-based results, it is clear that the number of traps should be considered to understand RTN characteristics. At least, multiple traps are the significant source of the large tail distribution of the RTN.

In addition, in this work, the dependence on trap position in the tunnel oxide thickness direction is investigated for both the low and high cell V_{th} states, as shown Fig. 11. The $1 \times 1 \times 1 \text{ nm}^3$ negative volume charge is assumed as a charged trap in this simulation. The trap

is randomly placed 3 nm from the channel surface. The probability of determined trap depth position is uniformity for simplicity. Simulation conditions are the same as those for the Poisson distribution except for the trap depth position. From this figure, it is found that the ΔV_{th} distributions considering the trap position in the tunnel oxide thickness direction for both the low and high cell V_{th} states are narrower than that of no-considering and more similar to those obtained using the RTN model. The effect of changing the trap depth position is greater for the ΔV_{th} distribution in the high- ΔV_{th} region. The trap depth position is also one of the important factors for understanding RTN characteristics.

5. Conclusions

ΔV_{th} distributions are investigated focusing on the number of traps and trap position depth in a 30 nm NAND multi level flash memory by 3D Monte Carlo device simulation including RDF. As a way for setting trap number, the fixed single trap, fixed double traps and Poisson distribution are assumed in this work. ΔV_{th} tails for the fixed single trap are not broadly at high ΔV_{th} region compared with the measurement-based results. On the other hand, the ΔV_{th} tail distributions with the fixed double traps are broadly like that. Average ΔV_{th} values for both of the fixed single trap and double traps are higher than that since are not considered cells without traps. The ΔV_{th} distribution in the lowest cell V_{th} state is the broadest among all cell states because channel current concentrates on the channel surface. Therefore, a high ΔV_{th} exists in the lowest cell V_{th} state since the trap is located at the channel surface. Moreover, the ΔV_{th} distribution with the number of traps along the Poisson distribution is investigated. Since no trap cells are considered in this trap, The average ΔV_{th} is markedly close to measurement-based results. It is found that the number of traps should be considered to understand RTN characteristics. The trap position in the tunnel oxide thickness direction is investigated. As a result, this factor was found to affect the ΔV_{th} distribution in the high- ΔV_{th} region for both the low and high cell V_{th} states and to be similar to measurement-based results.

Acknowledgments

This work is partly supported by JSPS KAKENHI Grant Number 25820148. The authors

thank the TCAD academic committee and Professor Hiramoto for help and discussions.

References

- 1) K. Fukuda, Y. Shimizu, K. Amemiya, M. Kamoshida, and C. Hu, IEDM Tech. Dig., 2007, p. 169.
- 2) K. Takeuchi, T. Nagumo, S. Yokogawa, K. Imai, and Y. Hayashi, Symp. VLSI Tech. Dig., 2009, p. 54.
- 3) A. Ghetti, C. M. Compagnoni, A. S. Spinelli, and A. Visconti, IEEE Trans. Electron Devices **56**, (2009) 1746.
- 4) S. M. Joe, M. K. Jung, W. Lee, M. S. Lee, B. S. Jo, J. H. Bae, S. K. Park, K. R. Han, J. H. Yi, G. S. Cho, and J. H. Lee, Symp. VLSI Tech. Dig., 2011, 112.
- 5) C. M. Compagnoni, A. S. Spinelli, S. Beltrami, M. Bonanomi, and A. Visconti, IEEE Electron Device Lett **29**, (2008) 941.
- 6) C. M. Compagnoni, R. Gusmeroli, A. S. Spinelli, and A. Visconti, IEEE Trans. Electron Devices, **55**, (2008) 3192.
- 7) A. Ghetti, C. M. Compagnoni, F. biancardi, A. L. Lacaita, S. Beltrami, L. Chiavarone, A. S. Spinelli, and A. Visconti, IEDM Tech. Dig., 2008, 1.
- 8) A. Ghetti, S. M. Amoroso, A. Mauri, and C. M. Compagnoni, IMW Tech. Dig., 2011, 1.
- 9) A. Ghetti, S. M. Amoroso, A. Mauri, and C. M. Compagnoni, IEEE Trans. Electron Device **59**, (2012) 309.
- 10) T. Nagumo, K. Takeuchi, T. Hase and Y. Hayashi, IEEE IEDM Tech. Dig., 2010, p.28.3.1
- 11) N. Tega, H. Miki, T. Osabe, A. Kotabe, K. Otsuga, H. Kurata, S. Kamohara, K. Tokami, Y. Ikeda, and R. Yamada, IEDM Tech. Dig., 2006, 1.
- 12) T. Kim, D. He, R. Porter, D. Rivers, J. Kessenich, and A. Goda, IEEE Electron Device Lett **31**, (2010) 153.
- 13) T. Kim, N. Franklin, C. Srinivasan, P. Kalavade, and A. Goda: IEEE Electron Device Lett **32**, (2011) 1183.
- 14) M. K. Jeong, S. M. Joe, H. J. Kang, K. R. Han, G. Cho, S. K. Park, B. G. Park, and J. H. Lee, Symp. VLSI Tech. Dig., 2013, T154.
- 15) E. Nowak, J. H. Kim, H. Y. Kwon, Y. G. Kim, J. S. Sim, S. H. Lim, D. S. Kim, K. H. Lee, Y. K. Park, J. H. Choi, and C. Chung, Symp. VLSI Tech. Dig., 2012, 21.
- 16) T. Tomita and K. Miyaji, Jpn. J. Appl. Phys **54**, (2015), 04DD02
- 17) Y. Li, C. H. Hwang, T. Y. Li, and M. H. Han, IEEE Trans. Electron Devices **57**, (2010)

437

- 18) Y. Li, S. M. Yu, J. R. Hwang, and F. L. Yang, *IEEE Trans. Electron Devices* **55**, (2008) 1449.
- 19) S. Markov, A. S. M. Zain, B. Cheng, and A. Asenov, *SOI Conf.*, (2012), 1.
- 20) A. Asenov, *IEEE Trans. Electron Devices* **45**, (1998) 2505.
- 21) A. Torsi, Y. Zhao, H. Liu, T. Tanzawa, A. Goda, P. Kalavade, and K. Parat, *IEEE Trans. Electron Devices* **58**, (2011) 11.
- 22) K. D. Suh, B. H. Suh, Y. H. Lim, J. K. Kim, Y. J. Choi, Y. N. Koh, S. S. Lee, S. C. Kwon, B. S. Choi, J. S. yum, J. H. Choi, J. R. Kim, and H. K. Lim, *IEEE J. Solid-State Circ* **30** (1995) 1149.
- 23) J. D. Lee, C. K. Lee, M. W. Lee, H. S. Kim, K. C. Park and W. s. Lee, *IEEE NVSMW* **21**, (2006) 31.
- 24) Y. Taur, G. J. Hu, R. H. Dennand, L. M. Terman, Y. T. Chung, and K. E. Petrillo, *IEEE Trans. Electron Devices* **32**, (1985) 203.
- 25) R. R. Troutman, *IEEE J. Solid-State Circuits* **14**, (1979) 383.
- 26) R. H. Dennard, F. H. Gaensslen, V. L. Rideout, and E. Bassous, *IEEE Solid-State and Integrated Circuits* **9**, (2003) 256.
- 27) D. Hisamoto, W. C. Lee, J. Kedzierski, and H. Takeuchi, *IEEE Trans. Electron Devices* **47**, (2002) 2320.
- 28) Z. H. Liu, H. Chenming, J. H. Huang, T. Y. Chan, M. C. Jeng, P. K. Ko, and Y. C. Cheng, *IEEE Trans. Electron Devices* **40**, (2002) 86.
- 29) S. Tanakamaru, C. Hung, A. Esumi, M. Ito, K. Li, and K. Takeuchi, *ISSCC Tech. Dig.*, 2011, 204.
- 30) D. Kang, S. Lee, H. M. Park, D. J. Lee, J. Kim, J. Seo, C. Lee, C. Song, C. S. Lee, H. Shin, J. Song, H. Lee, J. H. Choi, and Y. H. Jun: *Symp. VLSI Tech. Dig.*, 2011, 206.

Figure Captions

Fig. 1 (Color online) Drain current I_D vs control gate voltage V_{CG} characteristics for trapped and detrapped state RTNs. ΔV_{th} is defined as RTN amplitude.

Fig. 2 (Color online) ΔV_{th} distributions considering fixed single trap and RDF at various N_A values. (a) Low N_A , (b) High N_A .

Fig. 3 (Color online) Simulated 30 nm NAND flash memory cell structure. (a) Overall cell structure view, (b) cross-sectional view of channel gate length L_g direction at the center of channel width W , and (c) cross sectional view of W direction at the center of L_g .

Fig. 4 (Color online) V_{th} distribution and corresponding data symbols in MLC NAND flash memory.¹³⁾ V_{th} and initial amount of charge in FG for each program state used in this work are also shown.

Fig. 5 (Color online) Probability of number of traps along Poisson distribution for each N_{trap} . (a) $N_{trap} = 2 \times 10^{10} \text{ cm}^{-2}$ and (b) $N_{trap} = 2 \times 10^{11} \text{ cm}^{-2}$.

Fig. 6 (Color online) ΔV_{th} distribution for (a) fixed single trap case and (b) fixed double traps in each cell V_{th} state.

Fig. 7 (Color online) Current density profiles at the channel center ($x = 0 \text{ nm}$) near (a) the lowest cell V_{th} state and (b) the highest cell V_{th} state.

Fig. 8 (Color online) Channel depth dependence on the channel current near cell V_{th} in the (a) lowest cell V_{th} state and (b) highest cell V_{th} state.

Fig. 9 (Color online) Spatial ΔV_{th} distribution along trap position along y for double traps in the (a) lowest cell V_{th} state and (b) highest cell V_{th} state. On the other hand, trap positions along the channel length direction x are fixed to 11 nm from the source edge where ΔV_{th} is highest.¹⁰⁾

Fig. 10 (Color online) ΔV_{th} distribution for Poisson distribution with (a) $N_{\text{trap}} = 2 \times 10^{10} \text{ cm}^{-2}$ and (b) $N_{\text{trap}} = 2 \times 10^{11} \text{ cm}^{-2}$

Fig. 11 (Color online) Dependence of the trap position in tunnel oxide thickness direction on ΔV_{th} distribution.

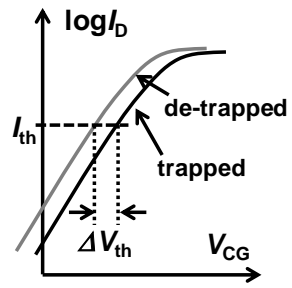


Fig. 1

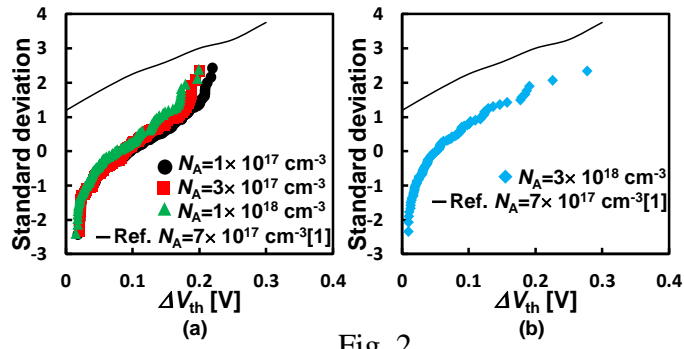


Fig. 2

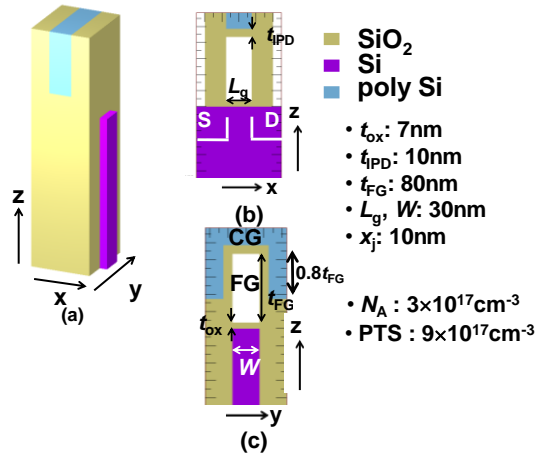


Fig. 3

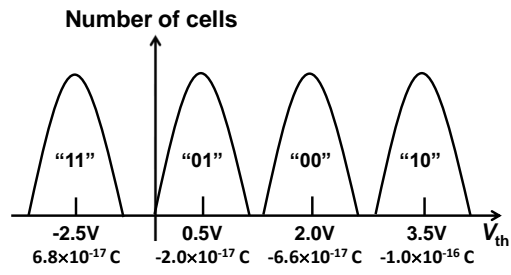


Fig. 4

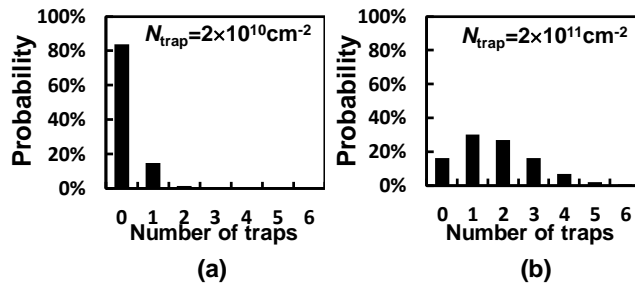


Fig. 5

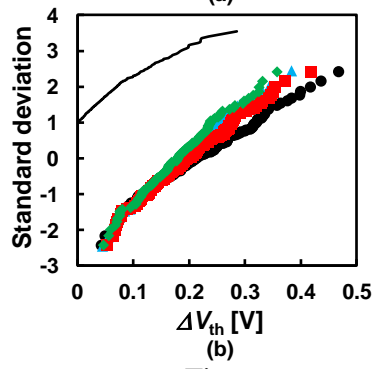
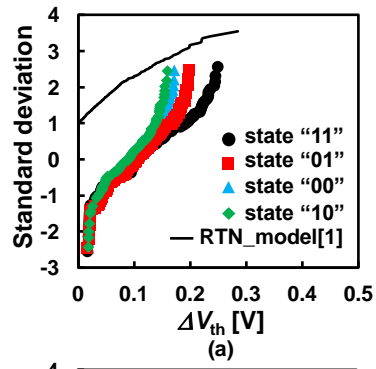


Fig. 6

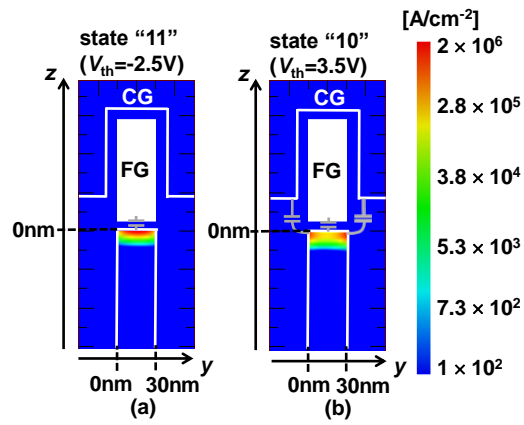


Fig. 7

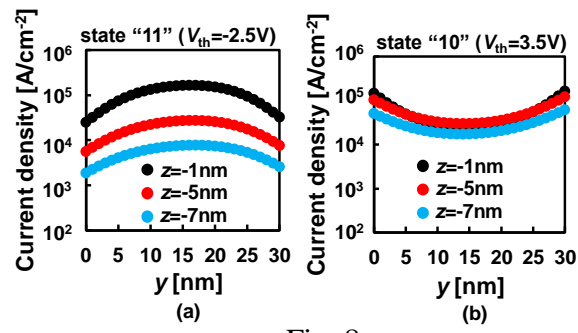


Fig. 8

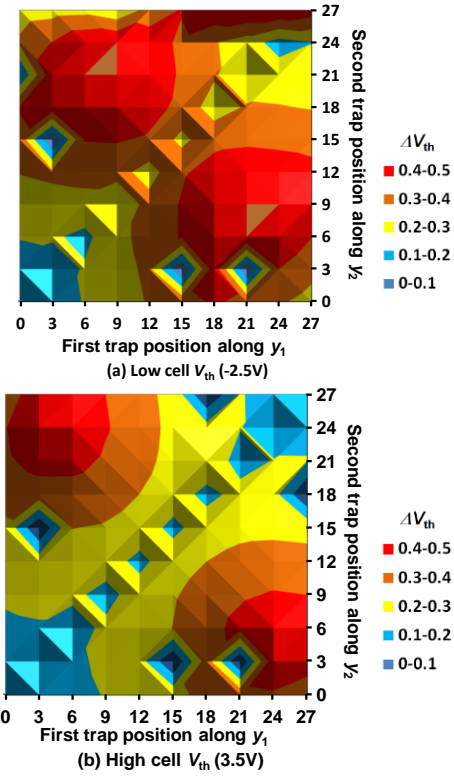
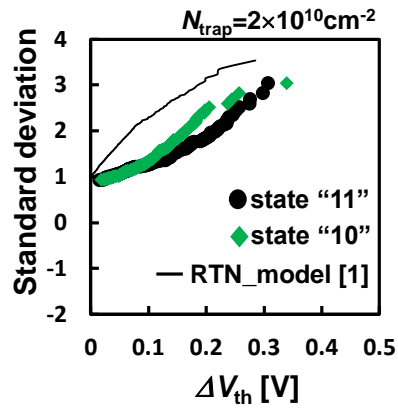
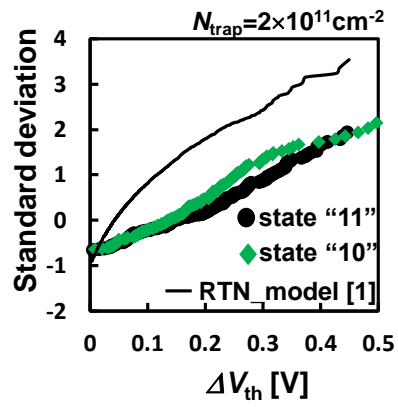


Fig. 9



(a) Low trap density



(b) High trap density

Fig. 10

- trap_depth_no_consider_state“11”
- trap_depth_no_consider_state“10”
- trap_depth_consider_state“11”
- trap_depth_consider_state“10”
- RTN_model [1]

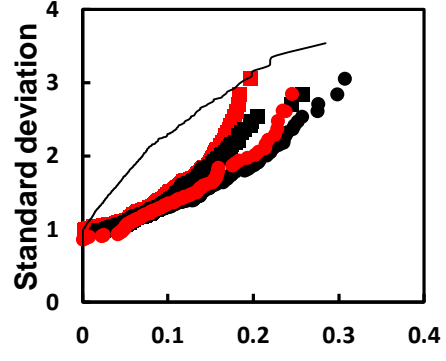


Fig. 11